ABSTRACT

An interconnect switch provides full PCI compatibility while increasing performance via concurrency. The switch contains a primary bridge on a primary port. Secondary ports of the switch can be connected to secondary bridges and end devices. The switch can shadow registers associated with the secondary bridges. A transaction with a target address behind a secondary bridge is directly routed to the secondary port associated with the secondary bridge, using the shadowed registers. A transaction with a target address not behind a secondary bridge is routed to each of the other secondary ports. The transaction can be broadcast to all of the non-bridge secondary ports or can be routed successively to each of the non-bridge secondary ports until accepted. A tuning process can use positive acknowledgment of a transaction by an end device connected to a secondary port to directly route similar transactions to the same secondary port.